BEE 271 Spring 2017
Homework 3 answers

Please answer the following questions. Each is worth 10 points.

1. What's the difference between a reg and a wire? If a variable isn't defined in Verilog, what does it default to?

   A reg remembers the value of the last assignment. A wire changes with whatever it's assigned to.

2. What is a vector in Verilog? If it's not a vector, what is it?

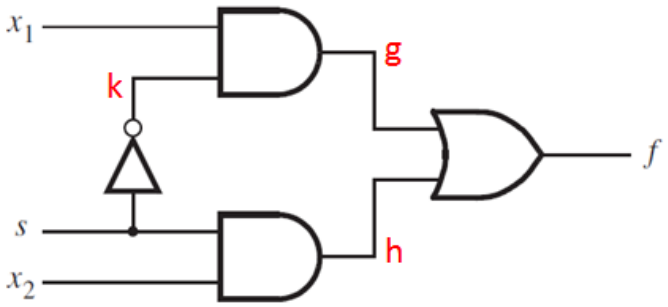
   A vector is multi-bit variable or value. If it's not a vector, it's a scalar, a one-bit variable or value.

3. What does { 2{ 4'h3 }, 2'b1 } equal? What is the { … } operation called?

   { 2{ 4'h3 }, 2'b1 } = 0011001101

   The { … } operator is the concatenation operator.

4. What does this circuit do? Is there a name for it? Write it as a Verilog module using only built-in gates and give it an appropriate name.



It's a multiplexer. It selects either x1 or x2 based on the value of s.

```
module Mux2to1( input x1, x2, s, output f );
   wire g, h, k;
   not( k, s );
   and( g, x1, k );
   and( h, s, x2 );
   or( f, g, h );
endmodule
```

5. Write the same function as a Verilog module using continuous assignment.

```
module Mux2to1( input x1, x2, s, output f );
   assign f = s ? x2 : x1;
endmodule
```

or

```
module Mux2to1( input x1, x2, s, output f );
   assign f = ( ~s & x1 ) | ( s & x2 );
endmodule
```

6. Write the same function as a Verilog module as a behavioral specification.

```
module Mux2to1( input x1, x2, s, output reg f );
   always @( * )
      if ( s )
         f = x2;
      else
         f = x1;
endmodule
```

7. What are three different ways to represent signed numbers in binary? Which method is commonly used, why is it preferred and how is it calculated?

   1. Sign + magnitude
   2. 1's complement
   3. 2's complement

   2's complement is preferred because numbers of opposite sign can be added without having to do a compare before (for sign + magnitude) or a correction after (for 1's complement).

8. What is the difference between carryout and overflow?

   Carryout is used with unsigned arithmetic and indicates a carry out of the MSB. Overflow is used with signed arithmetic and indicates a carry into the sign bit.

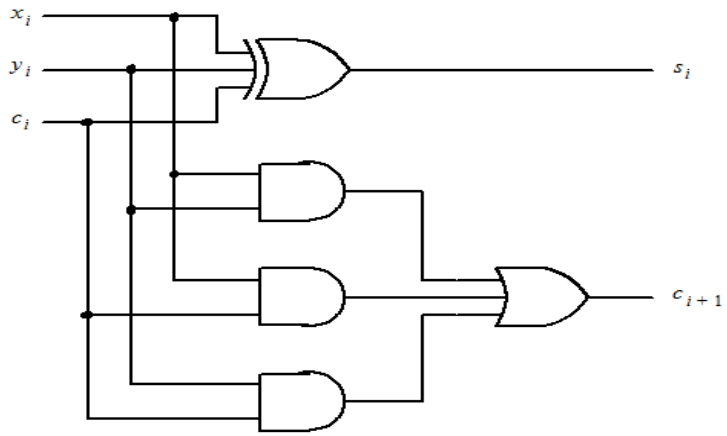
9. What's the difference between a half-adder and a full-adder? Draw the truth table and gate-level schematic for a full adder.

   A half-adder adds two bits and produces a sum and a carryout. A full-adder adds two bits plus a carryin.

Here's the truth table and an SOP implementation.

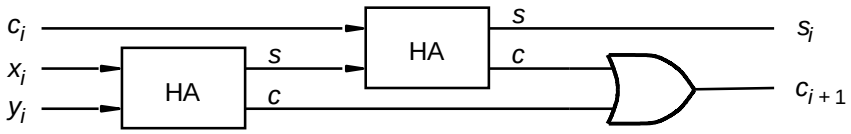
c_i	x_i	y_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a) Truth table

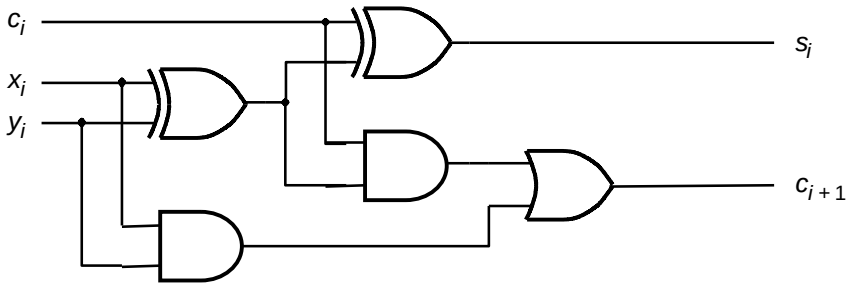


(c) Circuit

Alternately, the full adder can be constructed from two half-adders.



(a) Block diagram



(b) Detailed diagram

10. What is critical path delay?

It is the largest delay from operands being presented as inputs until all output bits are valid.